VIETNAM NATIONAL UNIVERSITY HANOI (VNU)

VNU UNIVERSITY OF ENGINEERING AND TECHNOLOGY

VENGME H.264/AVC – A Low Power 130nm H.264/AVC Compatible Video Encoder for Next Generation Multimedia Equipment

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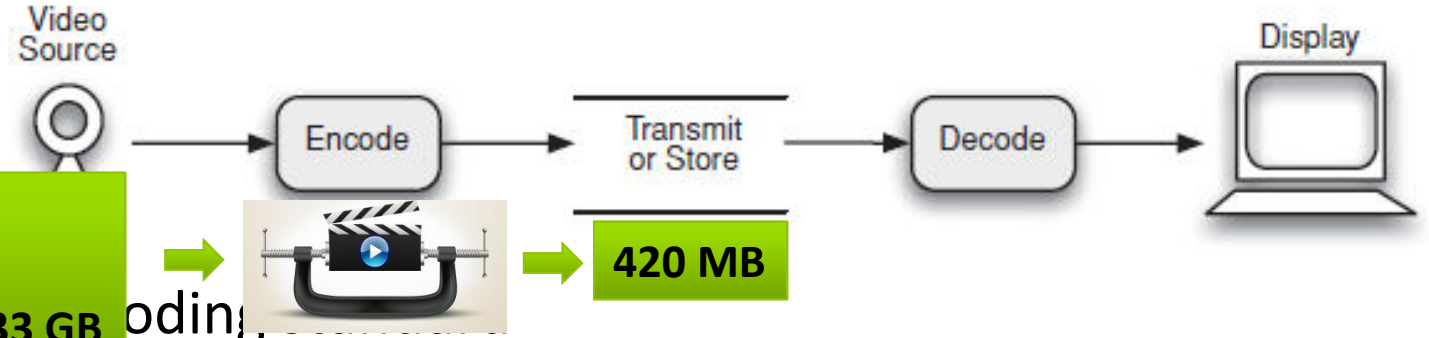
Key Laboratory for Smart Integrated Systems (SISLAB)

Outline

- Context and Motivation
- VENGME H.264/AVC: architecture, design, implementation
- FIFO-based low power method
- Conclusion & Perspective

Context: video coding

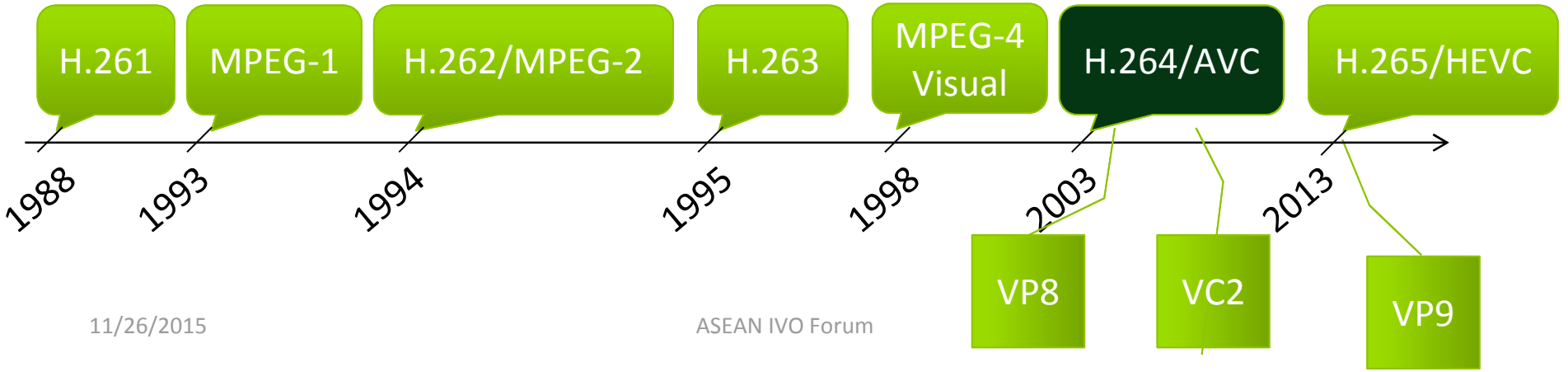
- Video coding



for 60 seconds
1080HD @ 25 fps
raw RGB 3x8 bit: **9.33 GB**

- oding
  - First specification version in May-2003, latest version in April-2013



H.264/AVC challenges

- ☑ Adopt wide set of video coding tools
- ☑ Provide significantly higher coding efficiency

  Achieves 39%, 49% and 64% of bit-rate reduction in comparison to MPEG-4, H.263 and MPEG-2

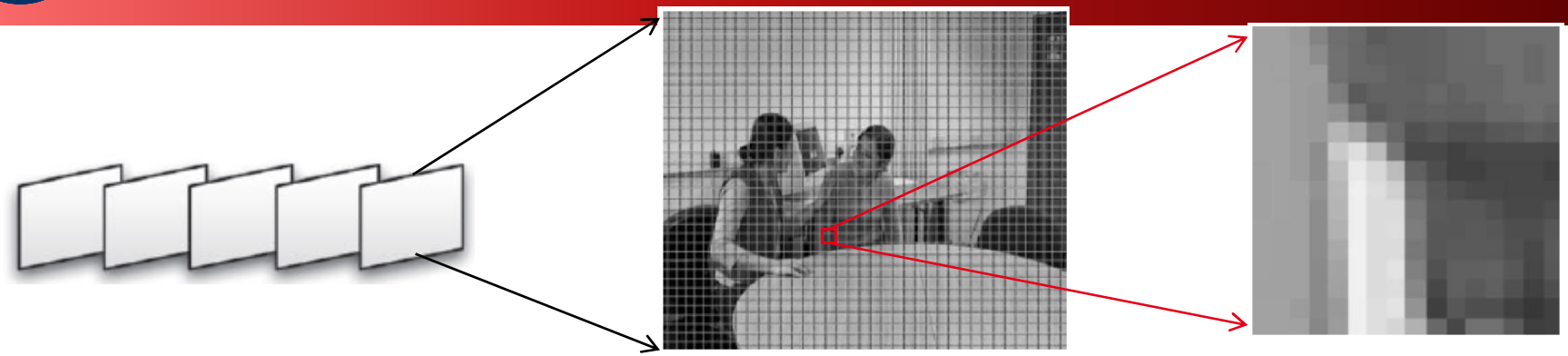
- ☑ Enable «network friendliness»
- ☑ Support variety applications

- ✖ High computational complexity & data dependency
- ✖ High power consumption

➔ **Hard to be implemented!**

➔ **Hardware designer need to reduce power consumption!**

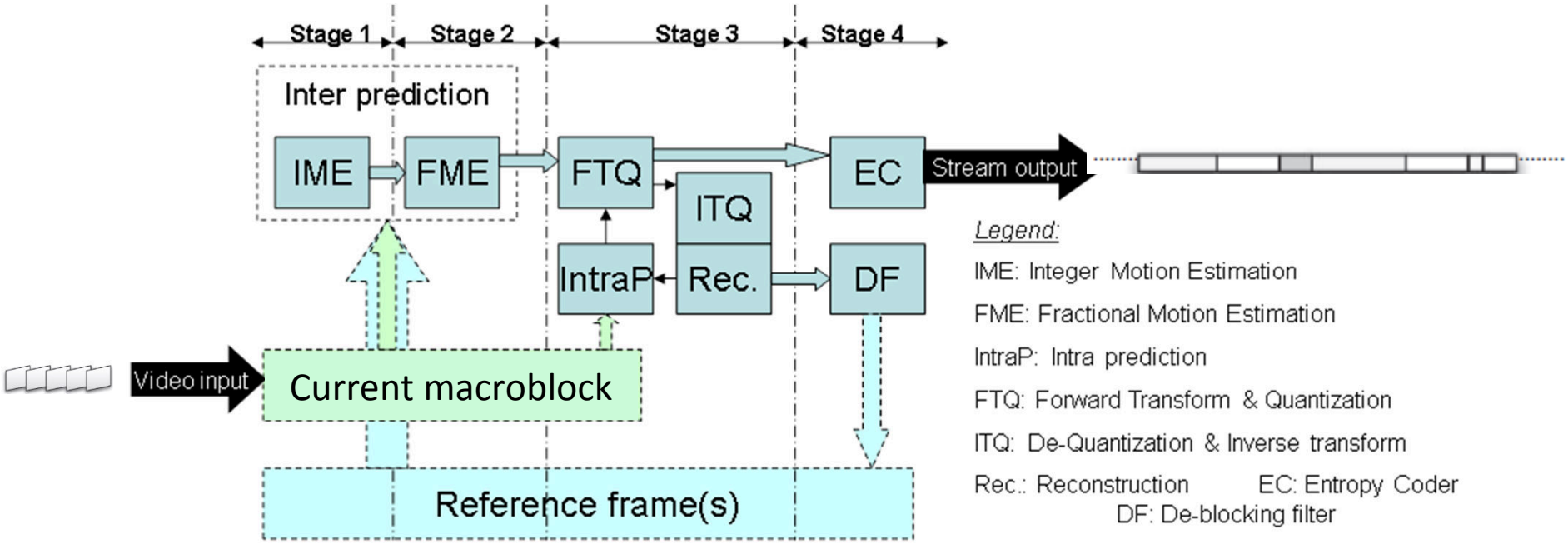
H.264/AVC encoding HW classical implementation



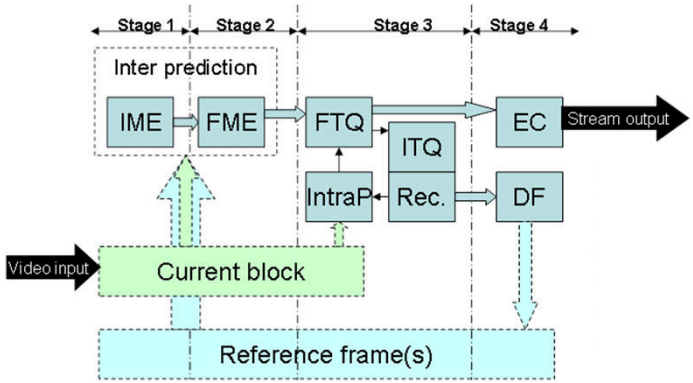
Video sequence

Video picture

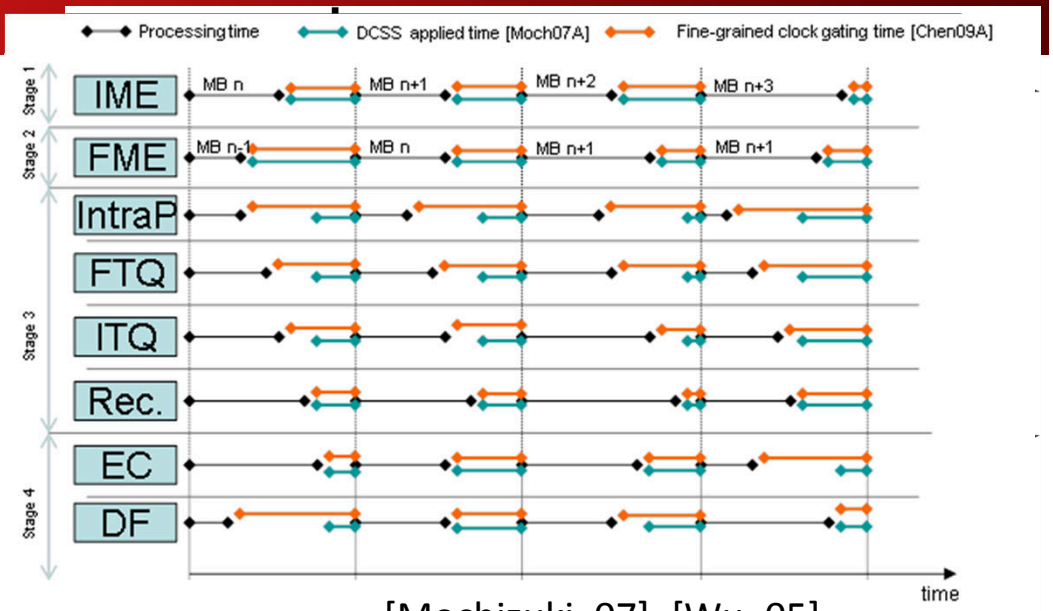
16×16-pixel macroblock



H.264/AVC encoding HW implementations



[Iwata, 09]



[Mochizuki, 07], [Wu, 05]

Scalability-oriented [Chen, 08] additional feature | high area cost

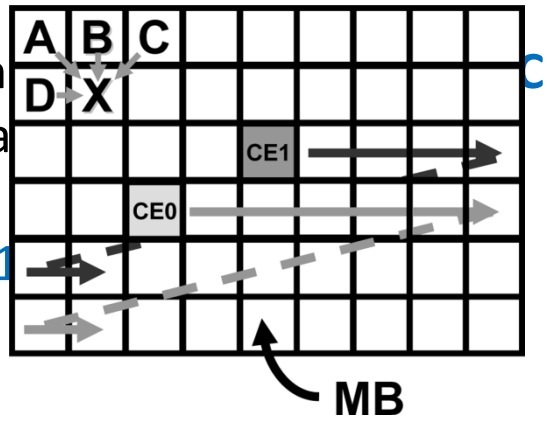
Speed-oriented [**Iwata, 09**] [Chen, 08] pipeline architecture for more parallelization | high area & power consumption cost

Power-oriented

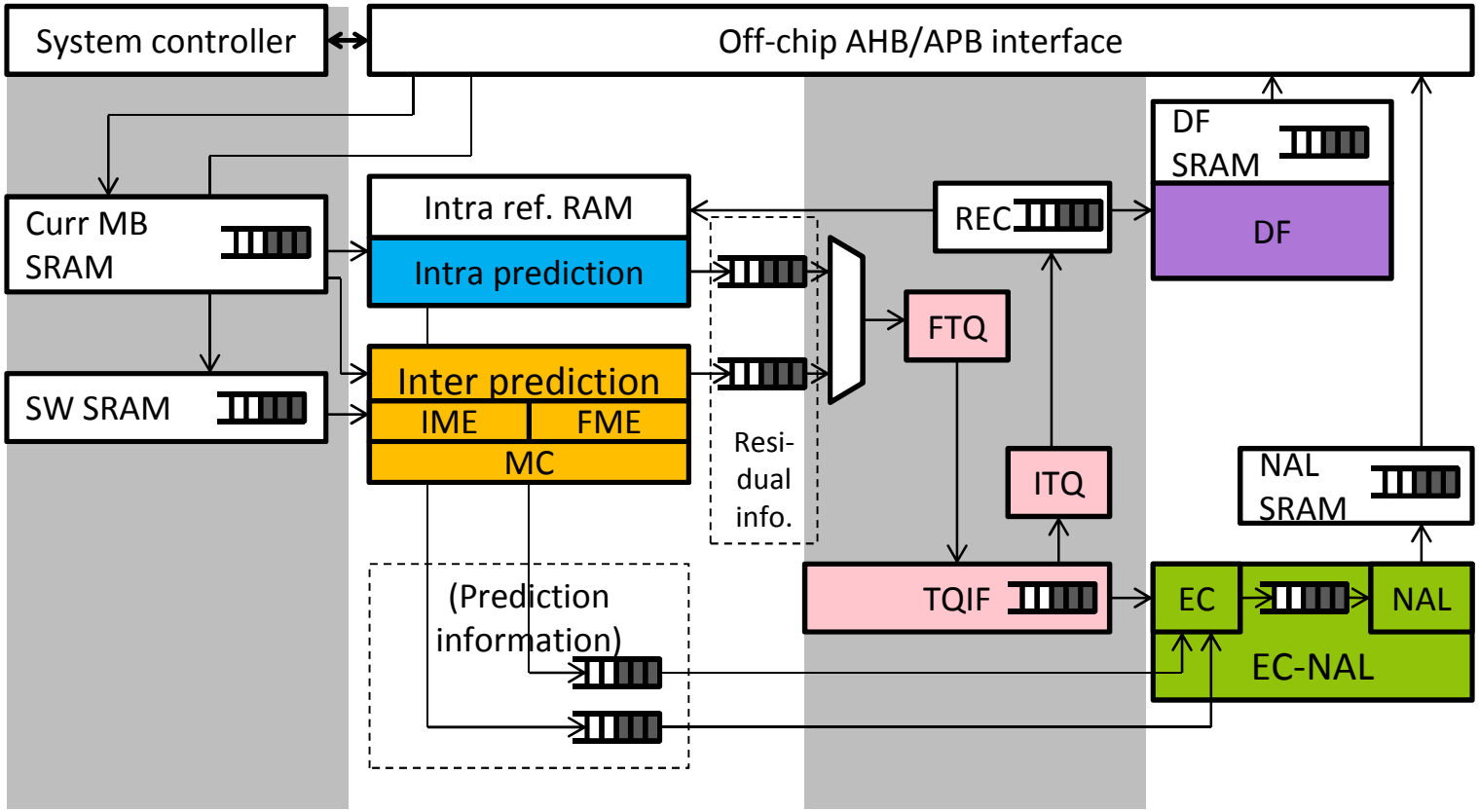
Dynamic Clock Supply Stop [**Mochizuki, 07**], fin **Chen, 09**]

Memory access reduction techniques applied a [Kim, 11][Lin, 08][Chen, 09]

Quality-scalability by parameterization [Kim, 11

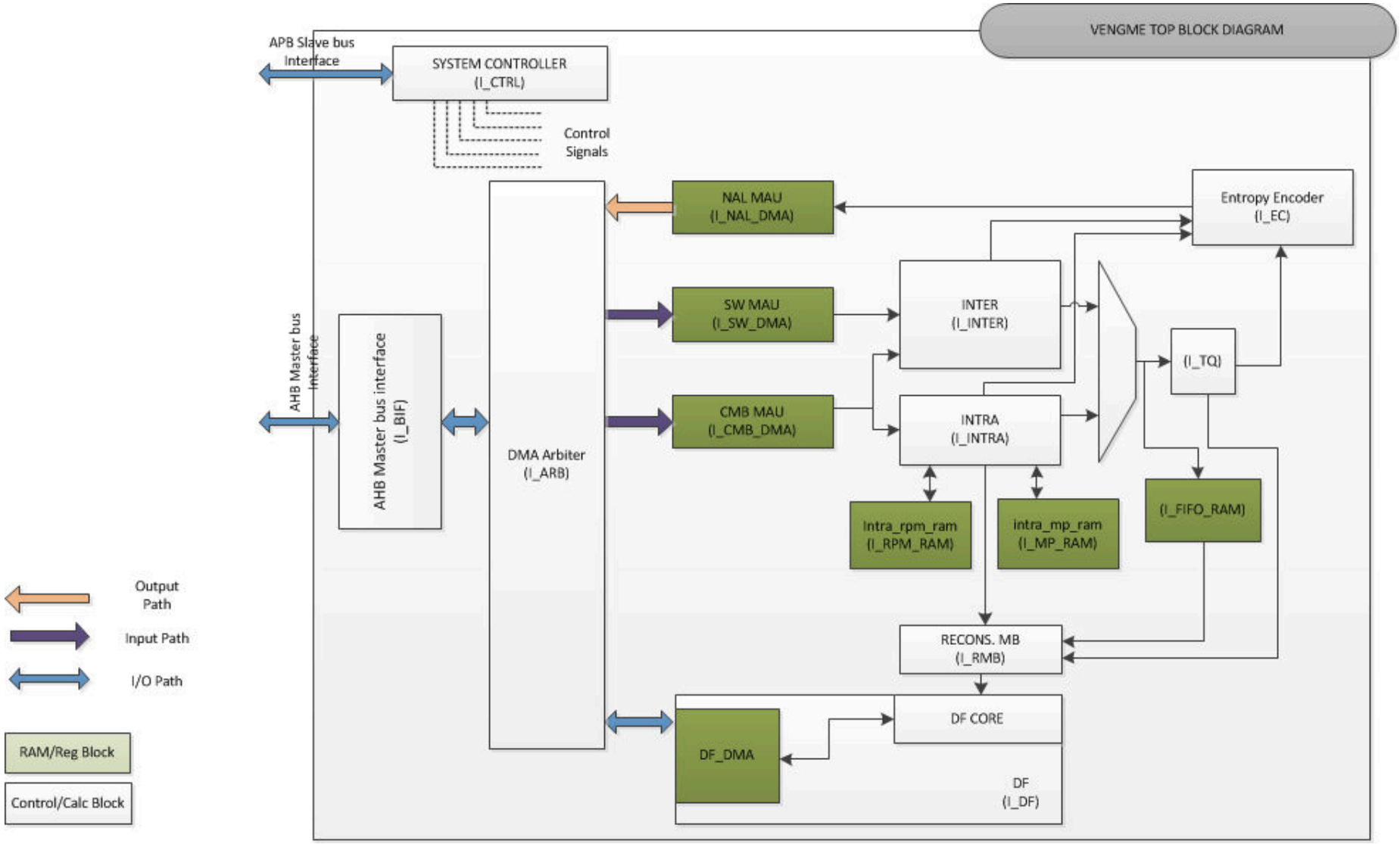


VENGME: 4-stage pipelining architecture



- 4-stage pipeline structure with low power design features
- **Main profile**: Maximal speed 11880MB/s, frame size 396MBs, bit rate 2Mbps

VENGME: System HW architecture (*simplified*)



VENGME: Specifications

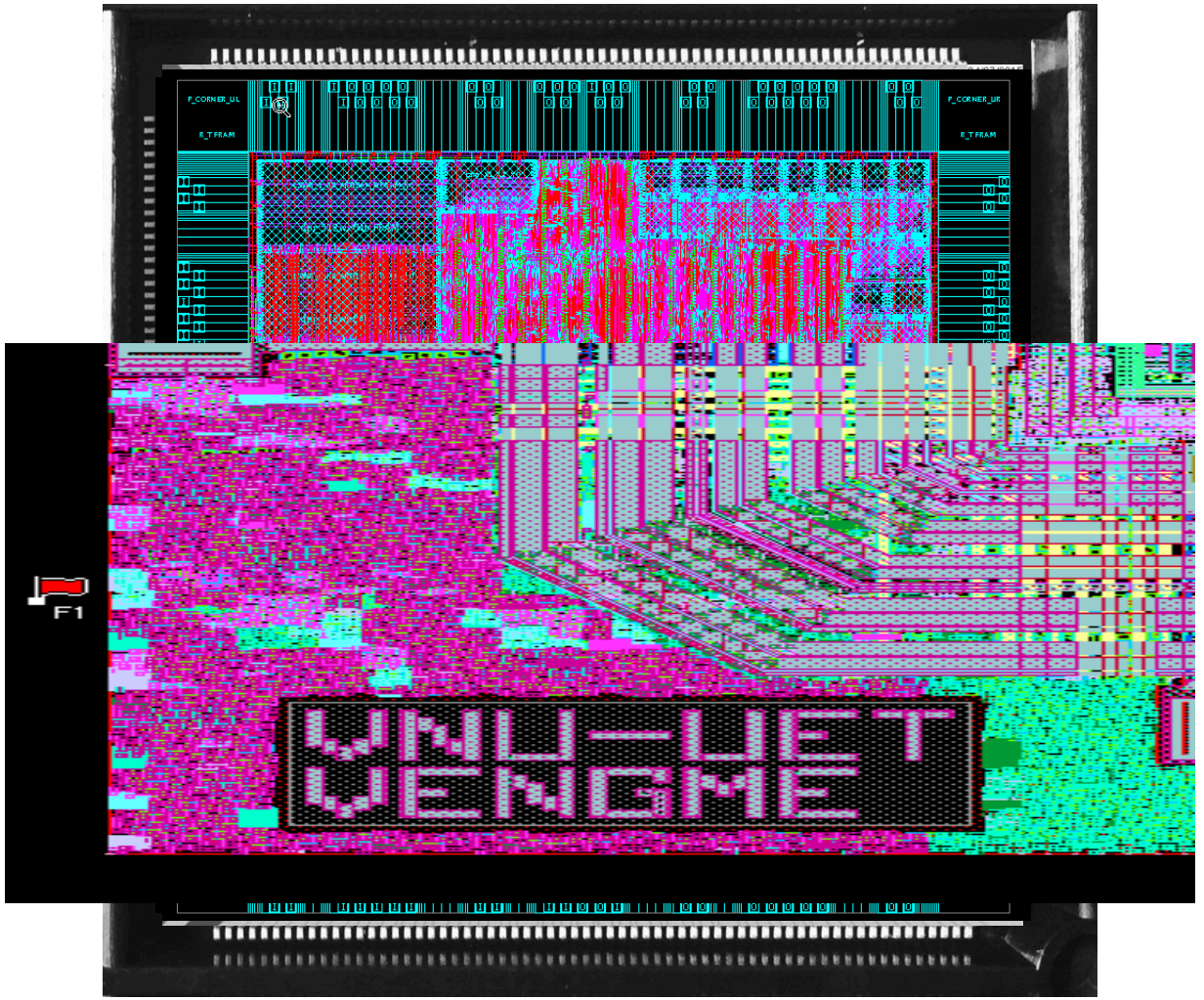
MAIN PROFILE

- Image format: QCIF/CIF **(up to HD 1280x720p@30fps)**
- Color sub-sampling: YUV 4:2:0 (progressive) with 8 bits/pixel
- Supporting I/P/B slices with configurable Group of Picture (GOP)
- System throughput (CIF sequences): 76 frames/s@100MHz
- Compression ratio: 2-70 times (depending on QP and Group of Pictures)
- Full-search inter prediction with variable block size partitioning
- Quarter-pixel accuracy and 48×48 search window size
- Full-search intra prediction
- CAVLC entropy coding with NAL bitstream formatting
- In-loop deblocking filters support
- Single transformation module with 4×4 FDCT/IDCT and 4×4, 2×2 Hadamard transform
- Objective quality: **PSNR: 24-64 dB** (depending on QP)
- **Power target: < 100mW**

VENGME: Key contributions

- An efficient HW architecture with **unbalance 4-stage pipeline processing** for developing power-aware ability;
- Memory access reduction by the proposed **data reuse mechanism**;
- **On-the-fly calculation** techniques ;
- **Low power techniques** (power gating, clock gating…);
- Optimization & pipelining techniques at block level.

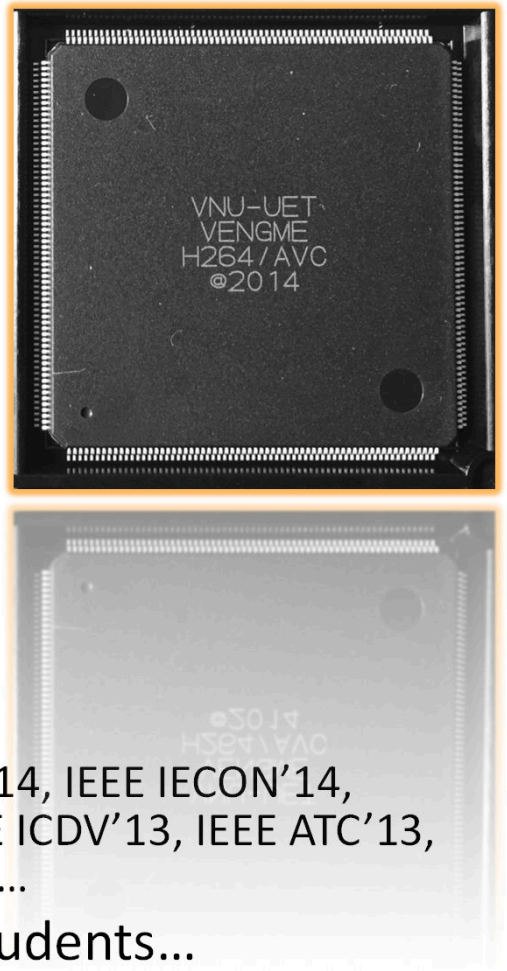
VENGME: test chip



VENGME: test chip

Features:

- Technology: Global Foundry CMOS 130nm
- Area overhead: 16mm^2
- Complexity: ~2 Mgates (with memory)
- Power consumption: 53mW
- Operating frequency: 100MHz
- Voltage: 1.2 volt
- Package: QFP256



Development:

- 18 man.year total investment for the chip design
  (completed and sent to Foundry in 2014)
- Publications: IEEE Trans. on VLSI (S), JEC'14, IEEE APCCAS'14, IEEE IECON'14, IEEE NEWCAS'14, IEEE DDECS'14, IEEE SOCC'13, REV'13, IEICE ICDV'13, IEEE ATC'13, ICGHIT'13, IEEE ATC'12, IEICE ICDV'12, JEC'11, IEEE DDECS'11…
- Training: 1 PhD student, 6 MSc students, 15 BSc students…
- 2 "Best Paper Awards"

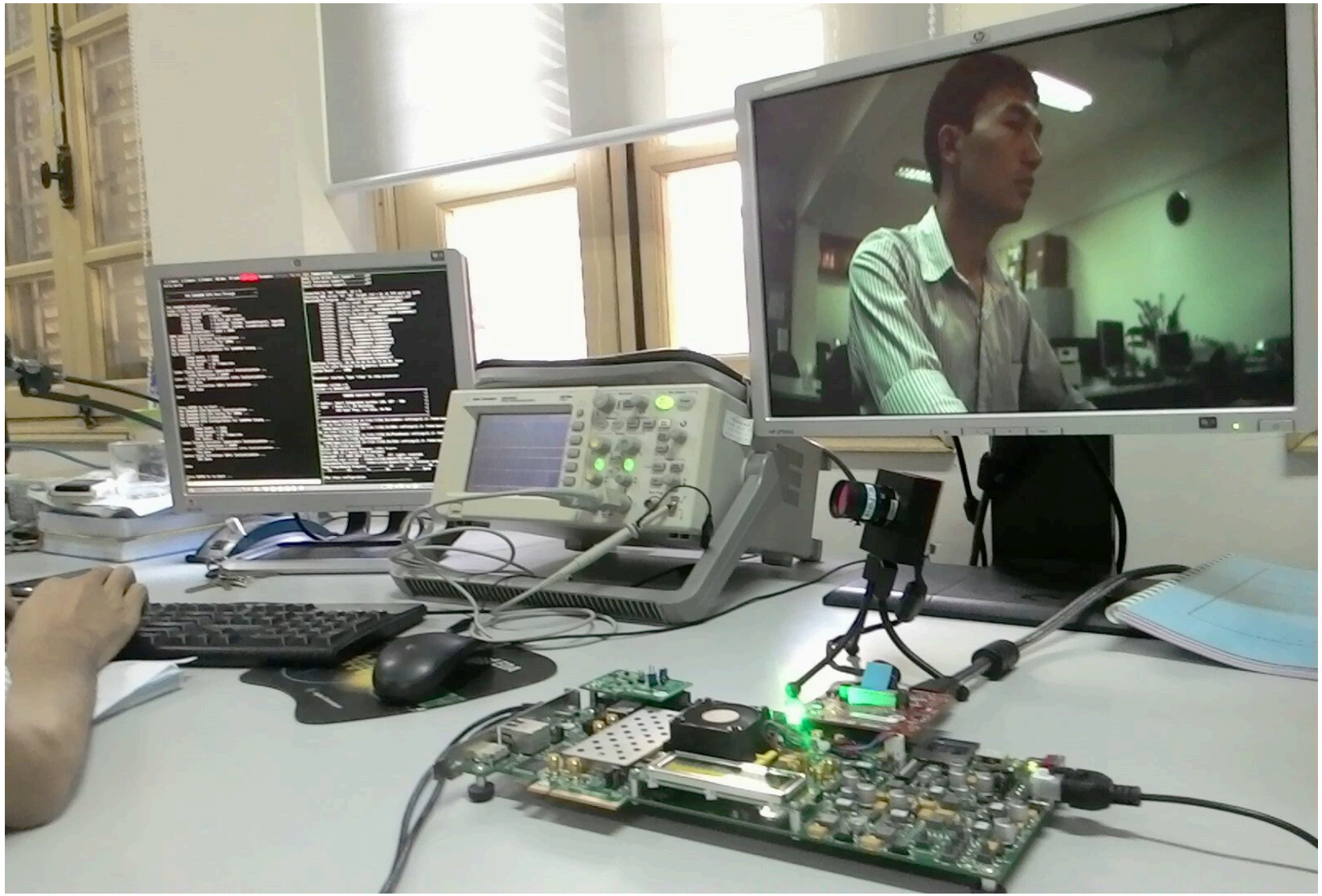
Comparison of VLSI H.264/AVC encoders

Design features	Z. Lui [1]	Y.-H. Chen [2]	K. Iwata [3]	T.-C Chen [4]	Y.-H Chen [5]	S. Mochizuki [6]	Y.-K. Lin [7]	H.-C Chang [8]	H. Kim [9]	VENGME H.264/AVC
Target	Real-time	SVC, high profile	Performance, Low power, Video size scalable	HW design for H.264 video codec	Low power, Low aware, Portable devices	Low power real-time high picture quality	High profile, Low area, High throughput	Dynamic Quality-Scalable, Power aware	Low power, Power aware	**Low power, real-time, portable devices**
Profile	Baseline, level 4	High profile, SVC	High, level 4.1	Baseline, level up to 3.1	Baseline	Baseline, level 3.2	Baseline/High level 4	Baseline	N/A	**Main Profile**
Resolution	1080p30	HDTV 1080p	1080p30	720p SD/HD	QCIF, 720SDTV	720p SD/HD	CIF to 1080p	CIF to HD720	CIF, HD 1280x720	**CIF, HD 720p (1280x720)**
Techno (nm)	UMC 180, 1P6M CMOS	UMC 90 1P9M	CMOS 65	UMC 180, 1P6M CMOS	TSMC 180, 1P6M CMOS	Renesas 90, 1POLY-7Cu-ALP	UMC 130	CMOS 130	N/A	**Global Foundry CMOS 130nm**
Frequency (MHz)	200	120(high profile); 166 (SVC)	162	81 (SD); 180 (HD)	N/A	54 (SD); 144 (HD	7.2 (CIF); 145 (1080p)	10-12-18-28 (CIF); 72-108 (HD720)	N/A	**100MHz (HD720p)**
Gate count (KGates)	1140	2079	3745	922.8	452.8	1300	593	470	N/A	**1900 (include memory)**
Memory (KBytes)	108.3	81.7	230	34.72	16.95	56	22	13.3	N/A	**N/A**
Power consumption (mW)	1410	360 (high profile), 411(SVC)	256	581(SD), 785(HD)	40.3(CIF, 2 references) 9.8-15.9(CIF 1 reference) 64.2(720SDTV)	64(720p HD)	6.74(CIF baseline), 242 (1080p high profile)	7-25(CIF), 122-183(HD720)	238.38 to 259.89 depends on PW level	**53mW (100MHz; HD720p)**

Demo (different encoded videos with different QPs)

PSNR > 30

Demonstration



Expected applications

Security

- Building management systems
- Public security systems
- Bank security systems
- School monitoring systems
- Govern… /military video conferencing

Internet of Things (IoT)

Trans…

VENGME H.264/AVC

Multimedia devices

- Monitoring cameras
- Intelligent transportation systems (ITS)

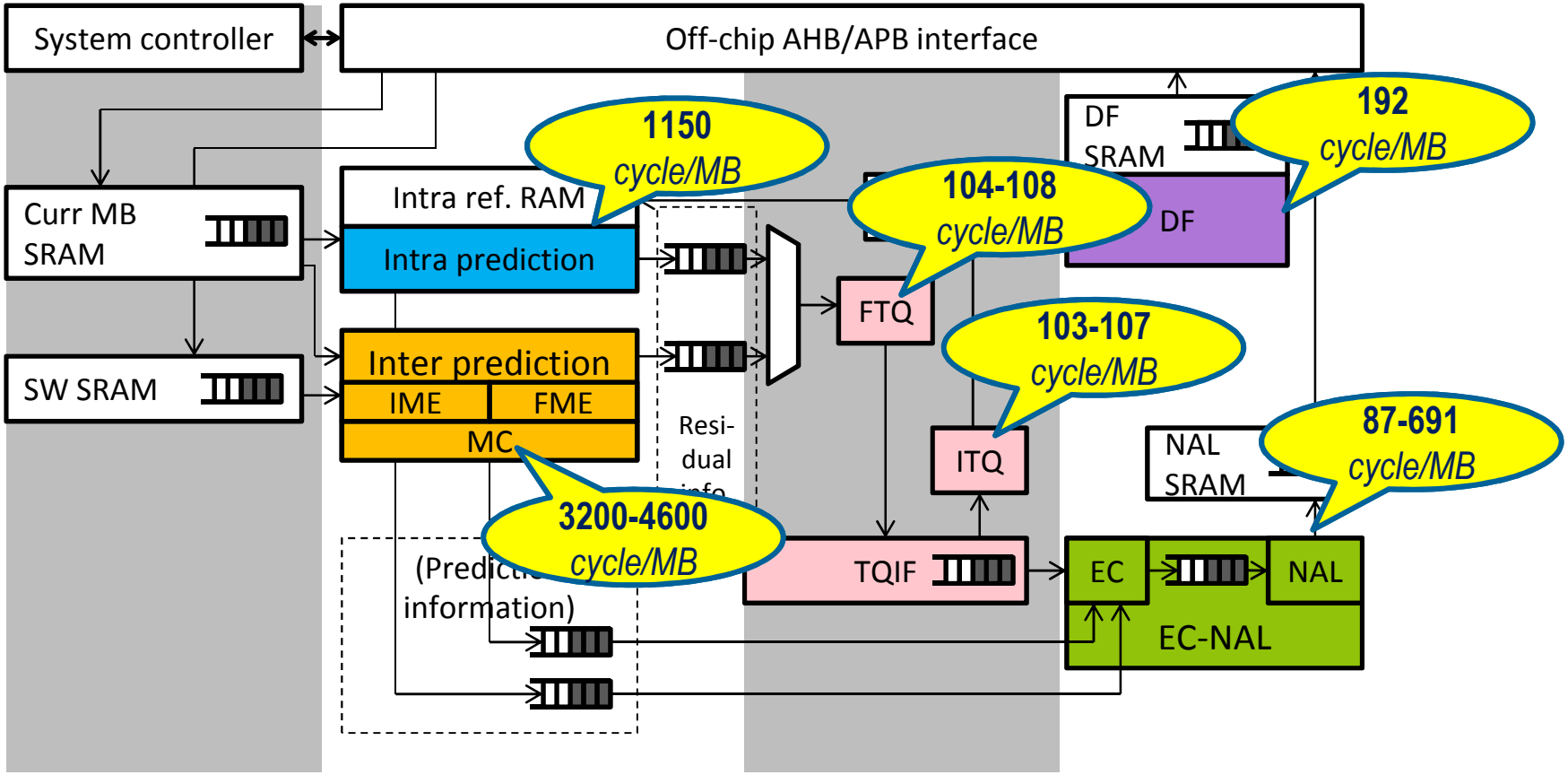
- Cameras, video recorder
- Mobile devices

Home use

- Security systems
- IP cameras

More power consumption techniques

- In VENGME: workload is not identical
  - Room to reduce power consumption

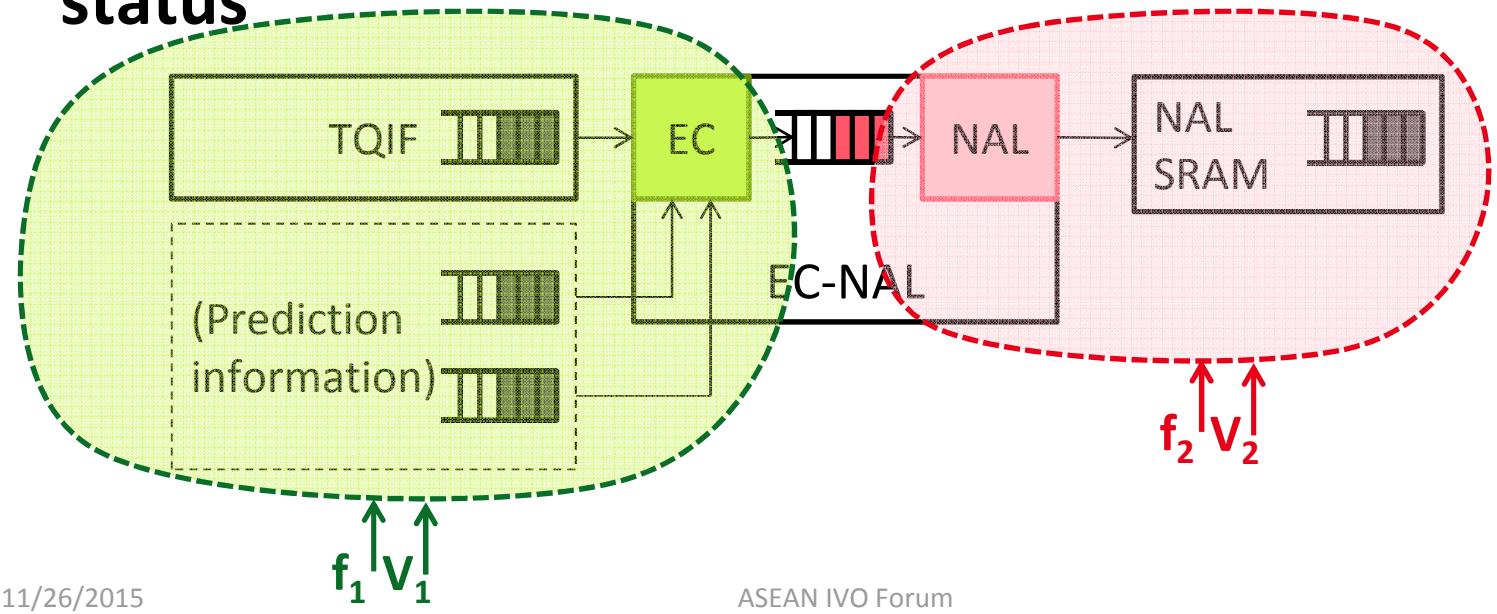


Power reduction method proposal

- Scale down (up) frequency (& voltage)
  - → power decrease (increase)

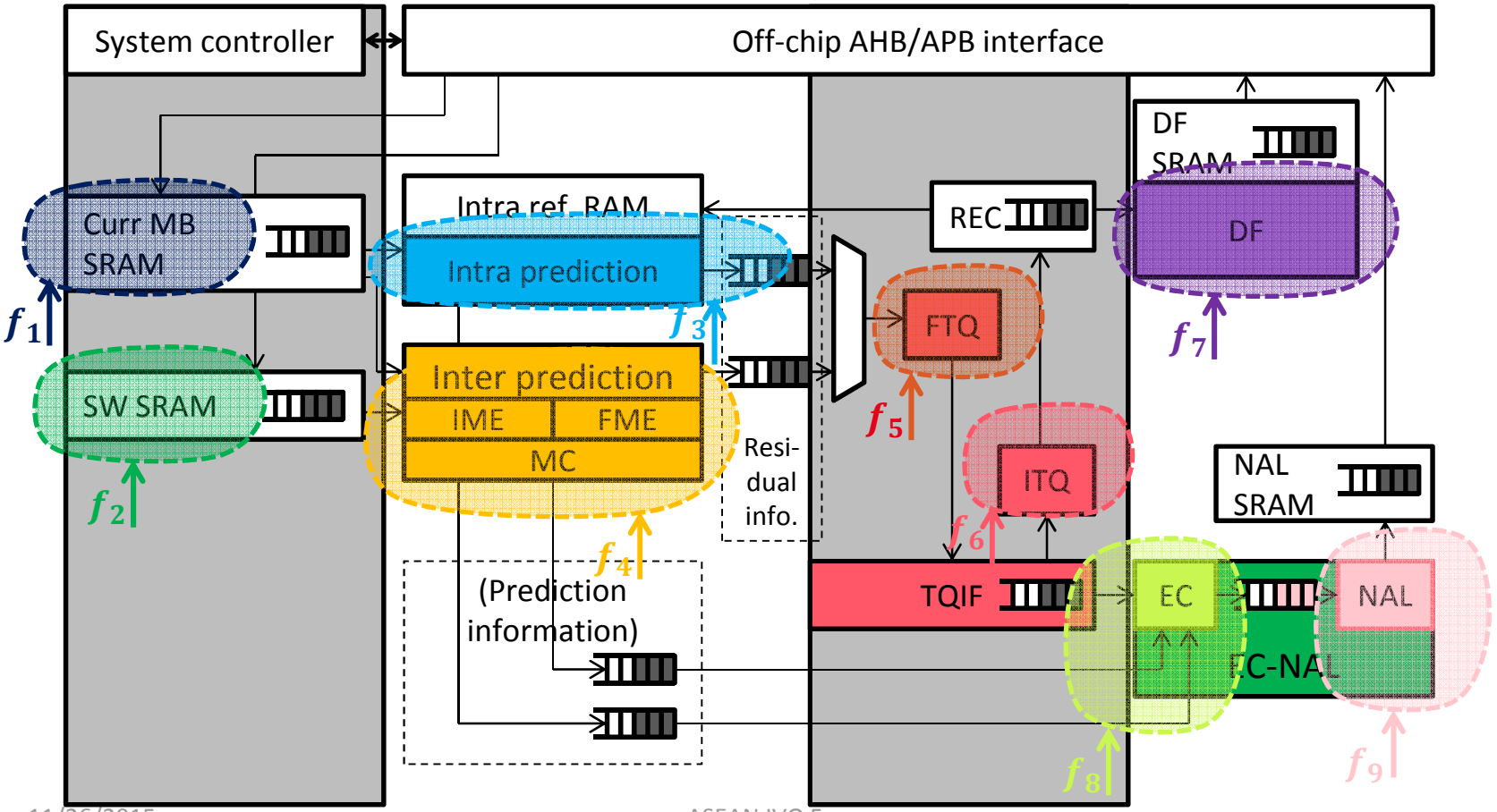
$$P_{total} = KC_L V_{dd}^{\ 2} f + q_{sc} f V_{dd} + I_{leakage} V_{dd}$$

  - → Smooth functioning of the FIFO
- Solution: Manage power consumption by scaling frequency *f* (and voltage *V*) according to **FIFO link status**



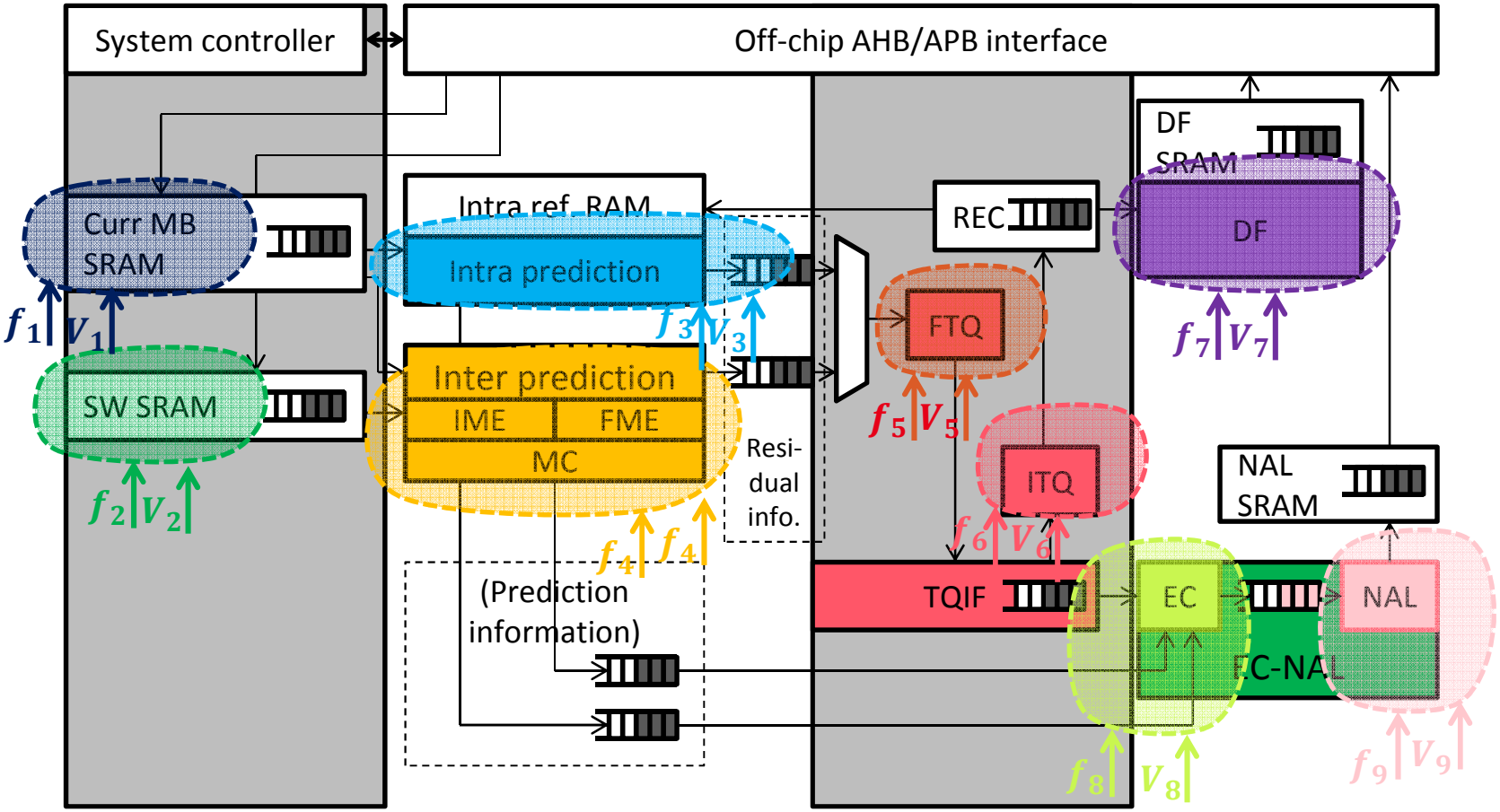
Perspectives

- Split in many frequency domains
  - Choosing the consuming module to apply the control
  - Global power optimization among controlled FIFOs



Perspectives

- Split in many power domains
  - Control law re-design
  - Delay due to power supply switching



Publications

- Nam-Khanh Dang, Alain Merigot, Xuan-Tu Tran. An Efficient Hardware Architecture for Inter-Prediction in H.264/AVC Encoders. IEEE Transactions on Very Large Scale Integration Systems.
- N.-M. Nguyen, et. al. An Overview of H.264 Hardware Encoder Architectures including Low Power Features. In REV Journal on Electronics and Communications (JEC), pp. 8-17, Vol. 4, No. 1-2, January - June, 2014, ISSN: 1859 – 387X.
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- N.-M. Nguyen, et. al. FIFO-level based Power Management and its Application to a H.264 Encoder. In Proceeding of the IEEE Industrial Electronics Conference , IECON14, pp. 158-163, Dallas, TX, USA, October 2014. (Best Presentation Award)
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